



UNITED STATES PATENT AND TRADEMARK OFFICE



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/008,696	11/08/2001	Jay B. Reimer	TI-30105	7469	
23494	7590 10/04/2004		EXAMINER		
TEXAS INSTRUMENTS INCORPORATED			DANG, KHANH		
P O BOX 655474, M/S 3999 DALLAS, TX 75265		ART UNIT	PAPER NUMBER		
, , , , , ,			2111		
			DATE MAILED: 10/04/2004	DATE MAILED: 10/04/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.



Application No. Applicant(s)	$-\mathcal{U}$
10/008,696 REIMER ET AL.	1
Office Action Summary Examiner Art Unit	
Khanh Dang 2111	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply	
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).	
Status	
1)⊠ Responsive to communication(s) filed on <u>04 August 2004</u> .	
2a)⊠ This action is FINAL . 2b)□ This action is non-final.	
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.	
Disposition of Claims	
 4) Claim(s) 1,3,5-8,10,13,14 and 17-19 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 5-8, 10, 13, 14, and 17-19 is/are allowed. 6) Claim(s) 1 and 3 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 	
Application Papers	
9)☐ The specification is objected to by the Examiner.	
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.	
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d) 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.).
Priority under 35 U.S.C. § 119	
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 	
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date. 5) Notice of Informal Patent Application (PTO-152)	
Paper No(s)/Mail Date S. Patent and Trademark Office TOL 326 (Rev. 1-04) Part of Paper No /Mail Date 2004003	

Application/Control Number: 10/008,696

Art Unit: 2111

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai et al. (Kawai).

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure that differs from Kawai.

With regard to claim 1, Kawai discloses a digital signal processing system, comprising: a plurality of processor subsystems (200) that each include: at least one memory device (100); and a memory bus multiplexer (in 108/400) coupled to each of said at least one memory device by a subsystem memory bus (152); and a direct memory access (DMA) controller (103), wherein each of the DMA controllers is coupled to each of said memory bus multiplexers and is configured to access each of said

Application/Control Number: 10/008,696

Art Unit: 2111

memory devices via the corresponding subsystem memory bus. See "Response to Applicants' argument" for discussion regarding to any newly added language to claim 1 by the amendment filed 8/4/2004.

With regard to claim 3, each of the plurality of processor subsystems (200) further includes: a host port interface (HPI) unit (including 401 and 402) coupled to the memory bus multiplexer (152) and configured to access the memory device via the subsystem memory bus. See "Response to Applicants' argument" for discussion regarding to any newly added language to claim 1 by the amendment filed 8/4/2004.

Response to Arguments

Applicants' arguments filed 8/4/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

Application/Control Number: 10/008,696

Art Unit: 2111

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

With regard to claim 1, Applicants argue that Kawai et al. does not disclose the limitation "each of the DMA controllers is coupled to each of said memory bus multiplexers of each of said plurality of processor subsystems." Contrary to Applicants' argument, it is clear from at least Figs. 6, 7, and 13 of Kawai et al., each memory controller (DMA 103) is coupled to of each of the memory bus multiplexers (108/400) of each processor subsystems (DSP 200). With regard to claim 3, Applicants argue that Kawai et al. fails to disclose the limitation "each host port interface is coupled to each memory bus multiplexer." Contrary to Applicants' argument, it is clear from at least Figs. 6, 7, and 13 of Kawai et al. that a host port interface (HPI) unit (including 401 and 402) coupled to the each memory bus multiplexer (152).

Allowable Subject Matter

Claims 5-8, 10, 13, 14, 17-19 are allowed.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2111

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang Primary Examiner